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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/675,974	09/29/2000	STAN W BOWLIN	F-316	1735

802 7590 08/11/2003

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EXAMINER	
LEE, CHRISTOPHER E	
ART UNIT	PAPER NUMBER
2189	7

DATE MAILED: 08/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/675,974	BOWLIN, STAN W	
	Examiner	Art Unit	
	Christopher E. Lee	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 8th of June, 2003. Claims 1, 8 and 9 have been amended; no claim has been canceled; and claims 10-19 have been newly added since the last Office Action was mailed on 12th of February, 2003. Currently, claims 1-19 are pending in this application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-19 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for transferring a first word (e.g., W3 at cycle 9 in Fig. 2) of RX_Data 34 (Fig. 2) on BUS 16 (Fig. 1) from MAC FIFO 14 (Fig. 1) to SDRAM 18 (Fig. 1) and DSP 20 (Fig. 1), i.e., supplying a second word of data (i.e., W5 at cycle 9) from the MAC FIFO to DSP as a read data operation (i.e., reading W5 at cycle 9 in Fig. 2 because of 2 clock cycles latency), and supplying said first word of data (i.e., W3) to SDRAM as a write data operation (i.e., writable W3 at cycle 9 in Fig. 2 because RX_Data has W3 at cycle 9; See Timing flow chart in Fig. 2), does not reasonably provide enablement for transferring a unit of data on a bus from a source to at least two destinations substantially simultaneously, i.e., supplying said unit of data from the source to first of said at least two destinations as a read data operation, and supplying said unit of data to a second of said at least two destinations as a write data operation, which is shown in claim 1 as an exemplary claim. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims. The Examiner doubts how to transfer a unit of data on a bus from a source to at least two destinations substantially simultaneously, i.e., even though a unit of data (e.g., reading W5 at cycle 9) of a read operation from MAC FIFO is not available on RX_Data on BUS at cycle 9, the claimed

invention substantially simultaneously executes a write operation of said unit of data (i.e., W5) to DSP, which is impossible to be implemented, because the Applicant admits that there are 2 clock cycles latency between a read data operation and a write data operation (See Fig. 2 and page 4, lines 23-24). Therefore, the Examiner assumes that the subject matter "a unit of data" or the like for a read operation is different from the subject matter "a unit of data" or the like for a write operation if both of the operations are performed substantially simultaneously for the claim rejection based on a prior art.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 10 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims recite respectively the limitation "said FIFO device" in line 1 of the claim 10, and in line 3 of the claim 11. There is insufficient antecedent basis for this limitation in the claim. Therefore, the term "said FIFO device" could be considered as --said FIFO data source-- since it is not clearly defined in the claims.

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1, 4-8, 12, 14-16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art [hereinafter AAPA] in view of Masterson et al. [US 5,073,851; hereinafter Masterson].

Referring to claim 1, AAPA discloses a method for transferring a first unit of data (e.g., byte or word depending on the read/write operation boundary alignment) on a bus (See page 2, line 34 through page 3, line 4) from a source (i.e., MAC) to at least two destinations (i.e., DSP and SDRAM), comprising

the steps of: supplying a second unit of data from said source (i.e., MAC) to first of said at least two destinations (i.e., DSP) as a read data operation (See page 2, line 35); and supplying said first unit of data to a second of said at least two destinations (i.e., SDRAM) as a write operation (See page 3, line 2). AAPA does not teach said first and second units of data transferring would been substantially simultaneously performed.

Masterson discloses an apparatus and method for improved caching in a computer system, wherein a first and second units of data transferring would been substantially simultaneously performed (See claim 1 and col. 5, lines 57-60; i.e., a read operation of a first unit of data (e.g., byte 2) is substantially simultaneously overlapped with a write operation of a second unit of data (i.e., byte 1)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of data transferring control (i.e., by the timing controller in gate array), as disclosed by Masterson, in said method of data transferring, as disclosed by AAPA, so as to pass said unit of data (i.e., byte 1, byte 2, byte 3, ... etc.) to said one of at least two destinations as a read operation, and to said other one of at least two destinations as a write operation substantially simultaneously with the advantage of speeding said operation of said transferring large amount of data (i.e., large blocks of information) during receiving data (i.e., during cache fill operation), which is disclosed at Masterson, col. 3, lines 60-65.

Referring to claim 4, AAPA teaches that at least one of said at least two destinations (i.e., SDRAM and DSP) comprise addressed data devices (i.e., SDRAM is a synchronous dynamic random access memory, which is accessed through an address bus, and DSP is a digital signal processor, which is accessing an external data through said address bus, too).

Referring to claim 5, AAPA teaches said at least one destinations comprises a microprocessor (i.e., DSP stands for Digital Signal Processor).

Referring to claims 6 and 7, AAPA teaches said at least one destinations comprises a memory storage, which is SDRAM (i.e., SDRAM stands for Synchronous Dynamic Random Access Memory).

Referring to claim 8, AAPA discloses an apparatus (i.e., network test device) for transferring received data in discrete units from a network (See page 2, line 34 through page 3, line 4), comprising: a bus (See page 3, line 1); a media access controller (i.e., MAC in page 2, line 35) for putting ones of discrete units of said received data from said network onto said bus (See page 2, lines 34-35); a microprocessor (i.e., DSP) for reading said ones of discrete units of data from said bus (See page 2, line 35); a memory (i.e., SDRAM) for writing said ones of discrete units of data from said bus into said memory (See page 3, line 2).

AAPA does not disclose a timing controller for controlling said media access controller, said microprocessor and said memory to have said media access controller write a first selected ones of discrete units of said data to said bus, said memory write said first selected ones of discrete units of said data to said memory and said microprocessor read a second selected ones of discrete units of said data substantially simultaneously.

Masterson discloses an apparatus and method for improved caching in a computer system, wherein a timing controller (i.e., gate array 34 of Fig. 2) for controlling (i.e., through cache memory control, main memory control and control lines from CPU in Fig. 2) a media access controller (i.e., main memory 15 of Fig. 2), a microprocessor (CPU 12 of Fig. 2) and a memory (i.e., cache 18 of Fig. 2) to have said media access controller (i.e., main memory) write a first selected ones of discrete units of said data (e.g., byte 1) to a bus (See col. 5, lines 45-54; i.e., wherein in fact that the DRAM controller provides an output enable signal to the main memory, then information in the main memory is accessed using addresses furnished by CPU implies that said media access controller (i.e., main memory) write data to a bus), said memory (i.e., cache) write said first selected ones of discrete units of said data (i.e., byte 1) to said memory (i.e., write access of the cache memory; See col. 5, lines 59-60) and said microprocessor (i.e., CPU) read a

second selected ones of discrete units of said data (i.e., byte 2 read access of the main memory, furnished by CPU) substantially simultaneously (i.e., reading access of main memory and writing access of cache memory are substantially simultaneously overlapped; See col. 5, lines 37-68).
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said timing controller, as disclosed by Masterson, in said apparatus, as disclosed by AAPA, so as to pass said data to said one of at least two destinations as a read operation, and to said other one of at least two destinations as a write operation substantially simultaneously with the advantage of speeding said operation of said transferring large amount of data (i.e., large blocks of information) during receiving data (i.e., during cache fill operation), which is taught by Masterson at col. 3, lines 60-65.

Referring to claim 12, Masterson teaches said supplying as a read and write operation of said units of data (i.e., byte 1, byte 2, byte 3, ... etc.) is accomplished with said units of data being presented on said bus as a single instance (i.e., byte).

Referring to claim 14, AAPA teaches said apparatus comprises a network test instrument (i.e., network test device; See page 2, lines 27, 28, and line 34 through page 3, line 3).

Referring to claim 15, Masterson teaches said memory (i.e., cache 18 of Fig. 2) write of said first selected quantity of data (i.e., byte 1) to said memory and said microprocessor read of said second selected quantity of data (i.e., byte 2) are accomplished with said first and second selected quantity of data being presented on said bus as a single instance (i.e., byte).

Referring to claim 16, AAPA discloses a method for operating a network test instrument (i.e., network test device; See page 2, lines 27, 28, and line 34 through page 3, line 3) to transfer data (i.e.., data in byte or word depending on the read/write operation boundary alignment) on a bus within said network test instrument (See page 2, line 34 through page 3, line 4) from a media access controller (i.e., MAC) at least to a processor (i.e., DSP) and to a memory, separate from said processor (i.e., SDRAM), comprising

the steps of : supplying said data from said media access controller (i.e., MAC) to said processor (i.e., DSP) as a read data operation performed by said processor (See page 2, line 35); and supplying said data to said memory (i.e., SDRAM) as a write operation (See page 3, line 2).

AAPA does not teach said step of supplying data to said processor and said step of supplying data to said memory are accomplished substantially simultaneously with use of the same transfer of said data on said bus.

Masterson discloses an apparatus and method for improved caching in a computer system, wherein step of supplying data (e.g., byte 2 of data) to a processor (i.e., CPU 12 of Fig. 2) and step of supplying data (i.e., byte 1 of data) to a memory (i.e., cache 18 of Fig. 2) are accomplished substantially simultaneously (i.e., reading access of main memory and writing access of cache memory are substantially simultaneously overlapped; See col. 5, lines 37-68) with use of the same transfer (i.e., overlapped transferring operation) of said data (i.e., said byte 1 and 2 are included in said data) on a bus (See claim 1 and col. 5, lines 57-60; i.e., a read operation of a first unit of data (e.g., byte 2) is substantially simultaneously overlapped with a write operation of a second unit of data (i.e., byte 1)). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of data transferring control (i.e., by the timing controller in gate array), as disclosed by Masterson, in said method of data transferring, as disclosed by AAPA, so as to pass said data (i.e., byte 1, byte 2, byte 3, ... etc.) to said one of at least two destinations as a read operation, and to said other one of at least two destinations as a write operation substantially simultaneously with the advantage of speeding said operation of said transferring large amount of data (i.e., large blocks of information) during receiving data (i.e., during cache fill operation), which is disclosed at Masterson, col. 3, lines 60-65.

Referring to claim 19, AAPA, as modified by Masterson, does not teach said units of data comprises a word.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented said units of data in word boundary alignment, such that said memory read/write operation and bus operation are based on said word boundary alignment, since it was known in the art that a memory access and bus operations in word boundary alignment is faster than a memory access and bus operation in byte boundary alignment.

Furthermore, it would have been an obvious matter of design choice to use said units of data in word, since the Applicant has not disclosed that said units of data in word solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with AAPA, as modified by Masterson.

7. Claims 2, 3, 9-11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Masterson [US 5,073,851] as applied to claims 1, 4-8, 12, 14-16 and 19 above, and further in view of DeSouza et al. [US 5,379,289 A; hereinafter DeSouza].

Referring to claim 2, AAPA, as modified by Masterson, discloses all the limitations of the claim 2 except that does not teach said source comprises a non-addressed data device.

DeSouza discloses a source (i.e., media access controller in Fig. 6) comprises a non-addressed data device (i.e., receiver FIFO 20 of Fig. 6; See col. 2, lines 5-14, wherein in fact that the data stored in the receiver FIFO is then transferred to a user system implies that said source (i.e., media access controller) comprises a receiver FIFO, which is a non-addressed data device since said stored data is transferred to said user system without being accessed by said user system).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said receiver FIFO, as disclosed by DeSouza, in said source (i.e., MCA), as disclosed by AAPA, as modified by Masterson, so as to transfer incoming data stream to said destinations (e.g., memory and processor) in succession (i.e., first-in-first-out sequence) with the advantage of

providing a buffering function, which is well known to one of ordinary skill in the art of digital circuit design.

Referring to claim 3, DeSouza teaches said source comprises a FIFO device (i.e., receiver FIFO 20 of Fig. 6).

Referring to claim 9, AAPA discloses an apparatus (i.e., network test device) for transferring data (See page 2, line 34 through page 3, line 4), comprising: a bus (See page 3, line 1); a data source (i.e., MAC in page 2, line 35) connected to said bus for putting data onto said bus (See page 2, lines 34-35); a microprocessor (i.e., DSP) connected to said bus for reading said data from said bus (See page 2, line 35); a memory (i.e., SDRAM) connected to said bus for writing said data from said bus into said memory (See page 3, line 2).

AAPA does not disclose a timing controller connected to said data source, said microprocessor and said memory for controlling said data source, said microprocessor and said memory to have said data source put said data onto said bus, and for a selected quantity of data, have said memory write said selected quantity of data to said memory and said microprocessor read said selected quantity of data substantially simultaneously.

Masterson discloses an apparatus and method for improved caching in a computer system, wherein a timing controller (i.e., gate array 34 of Fig. 2) connected to a data source (i.e., the gate array 34 is connected to the main memory 15 via the main memory control line and the main memory address line, shown in Fig. 2), a microprocessor (i.e., the gate array 34 is connected to the CPU 12 via the control lines, shown in Fig. 2) and a memory (i.e., the gate array 34 is connected to the cache 18 via the cache memory control line and the cache address line, shown in Fig. 2) for controlling (i.e., through cache memory control, main memory control and control lines from CPU in Fig. 2) said data source (i.e., main memory 15 of Fig. 2), said microprocessor (i.e., CPU 12 of Fig. 2) and said memory (i.e., cache 18 of Fig. 2) to have said data source (i.e., main memory) put said data onto said bus (See col. 5, lines 45-54; i.e., wherein

in fact that the DRAM controller provides an output enable signal to the main memory, then information in the main memory is accessed using addresses furnished by CPU implies that said data source (i.e., main memory) put data to said bus), and for a selected quantity of data (i.e., data, which consists of byte 1, byte 2, byte 3, ... etc.), have said memory (i.e., cache) write said selected quantity of data to said memory (i.e., write access of the cache memory; See col. 5, lines 59-60) and said microprocessor (i.e., CPU) read said selected quantity of data (i.e., read access of the main memory, furnished by CPU; See col. 5, lines 58-59) substantially simultaneously (i.e., reading access of main memory and writing access of cache memory are substantially simultaneously overlapped; See col. 5, lines 37-68).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said timing controller, as disclosed by Masterson, in said apparatus, as disclosed by AAPA, so as to pass said data to said one of at least two destinations as a read operation, and to said other one of at least two destinations as a write operation substantially simultaneously with the advantage of speeding said operation of said transferring large amount of data (i.e., large blocks of information) during receiving data (i.e., during cache fill operation). Refer to Masterson, col. 3, lines 60-65.

AAPA, as modified by Masterson, does not expressly teach said data source is a FIFO data source.

DeSouza discloses a data source (i.e., media access controller in Fig. 6) comprises a FIFO data source (i.e., receiver FIFO 20 of Fig. 6).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said receiver FIFO, as disclosed by DeSouza, in said data source (i.e., MCA), as disclosed by AAPA, as modified by Masterson, so as to transfer incoming data stream to said destinations (e.g., memory and processor) in succession (i.e., first-in-first-out sequence) with the advantage of providing a buffering function, which is well known to one of ordinary skill in the art of digital circuit design.

Referring to claim 10, AAPA, as modified by Masterson and DeSouza, teaches said data source (i.e., MAC in page 2, line 35; AAPA) including FIFO receiver (i.e., FIFO data source; AAPA, as modified by Masterson and DeSouza) is a media access controller (i.e., MAC).

Referring to claim 11, AAPA, as modified by Masterson and DeSouza, teaches said apparatus is a network test instrument, which is taught by AAPA at page 2, lines 27, 28, and line 34 through page 3, line 3, and said data source (i.e., MAC in page 2, line 35; AAPA) including FIFO receiver (i.e., FIFO data source; AAPA, as modified by Masterson and DeSouza) is a media access controller (i.e., MAC).

Referring to claim 13, AAPA, as modified by Masterson and DeSouza, teaches said source (i.e., MAC in page 2, line 35; AAPA) including FIFO receiver (i.e., FIFO data source; AAPA, as modified by Masterson and DeSouza) is a media access controller (i.e., MAC).

8. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Masterson [US 5,073,851] as applied to claims 1, 4-8, 12, 14-16 and 19 above, and further in view of IBM_TDB ["Circuit for Tracing Branch Instructions" by IBM Technical Disclosure Bulletin, December 1979, Vol. 22, Issue No. 7, pages 2651-2654].

Referring to claims 17 and 18, AAPA, as modified by Masterson, discloses all the limitations of the claims 17 and 18, respectively, except that does not teach determining whether said data, which is said unit of data, currently transferred to said memory, which is SDRAM, is to be retained before a next data (i.e., a next unit of data), is transferred said memory, and if said data currently transferred is to be retained, modifying a next write address location so that a next data does not overwrite said data currently transferred, and otherwise, if said data currently transferred is not to be retained in said memory, keeping said next data write address as a current data write address value so that said next data is written over said data currently transferred.

IBM_TDB discloses a tracing test system, wherein determining (i.e., by Branch Detect Circuit in Fig. 1) whether a data (i.e., instruction) currently transferred to a memory (i.e., Trace Memory in Fig. 1) is to be

retained before a next data is transferred said memory (See Disclosure Text, 2nd paragraph, lines 1-4), and if said data currently transferred is to be retained (i.e., if the current instruction is a branch instruction), modifying a next write address location so that a next data does not overwrite said data currently transferred (See Disclosure Text, 2nd paragraph, lines 8-14 and 17-19), and otherwise, if said data currently transferred is not to be retained in said memory, keeping said next data write address as a current data write address value so that said next data is written over said data currently transferred (See Disclosure Text, 2nd paragraph, lines 6-8 and 15-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method steps of tracing test system, as disclosed by IBM_TDB, in said method, as disclosed by AAPA, as modified by Masterson, so as to record said data (i.e., each instruction) operated on a network (i.e., executed by a processor) under test, for the advantage of generating an audit trail that is helpful in system debug (See Disclosure Text, 1st paragraph, lines 1-3).

Examiner's Note

9. *In response to the Applicant's note with respect to* Formal Drawings Requirement, the Applicant's statement is correct because the Formal Drawings Requirement statement on the Office Action mailed on 12th of February, 2003 (hereinafter the last Office Action) was in a typographical error. However, Formal drawings will be required when the application is allowed, and the typographical error didn't affect claim rejections in the last Office Action.

Response to Arguments

10. Applicant's arguments filed on 8th of June, 2003 have been fully considered but they are not persuasive.

11. *In response to the Applicant's argument with respect to* "Claims 1 and 4-8 rejected under 35 U.S.C. ... In the cited portion of Masterson et al, a read of data byte #2 is taking place at about the same time that a write of data byte #1 is happening. This is not what applicant claims. Applicant's invention

relates to supplying the same data substantially simultaneously to two different devices. One of those devices is accessing the data as a read operation, while the other is accessing the data as a write operation. ..." on Response page 7, line 12 through page 8, line 9, the Examiner respectfully disagrees. In contrary to the Applicant's statement, the Applicant's claimed invention cannot afford the feature, such that supplying the same data substantially simultaneously to two different devices, i.e., one of those devices is accessing the data as a read operation, while the other is accessing the data as a write operation because of the 2 clock cycles latency between said read operation and said write operation, which is clearly shown in the Figure 2, Timing flowchart in the application. For example, in case of transferring a word (e.g., W3 at cycle 9 in Fig. 2) of RX_Data 34 (Fig. 2) on BUS 16 (Fig. 1) from MAC FIFO 14 (Fig. 1) to SDRAM 18 (Fig. 1) and DSP 20 (Fig. 1), supplying said word of data (i.e., W3) to SDRAM as a write data operation (i.e., writable W3 at cycle 9 in Fig. 2 because RX_Data has W3 at cycle 9) is possible to be performed at cycle 9. However, supplying said word of data (i.e., W3 at cycle 9) from the MAC FIFO to DSP as a read data operation had been performed at cycle 7. At cycle 9, said read operation performs to read another word of data (i.e. W5). Therefore, the Applicant's claimed invention does not reasonably provide enablement for transferring a unit of data on a bus from a source to at least two destinations substantially simultaneously (See paragraph 2 of the instant Office Action, Claim Rejection - 35 USC § 112, first paragraph). Thus, the Applicant's argument on this point is not persuasive.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH

shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Christopher E. Lee
Examiner
Art Unit 2189

cel/ CEL
August 6, 2003

Sumati Lefkowitz
SUMATI LEFKOWITZ
PRIMARY EXAMINER